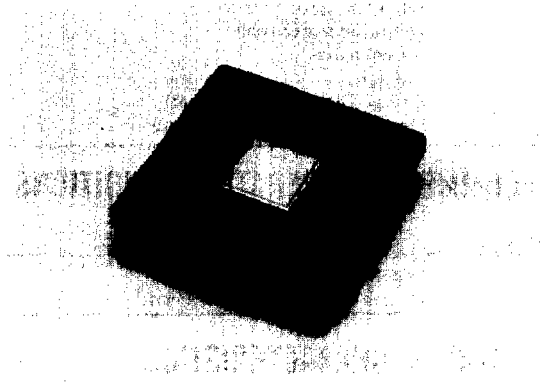
ANALOG DEVICES

TTL 16 × 16-Bit Multiplier

ADSP-7018

FEATURES
16 × 16-bit Parallel Multiplication
19ns Max Multiplication Time
TTL Compatible
4.0W Max Power Dissipation
Independent Input and Output Latches Which Can Be Made Transparent
Unclocked, Single-, Double-, and Triple-Clock Operation
Twos Complement, Unsigned Magnitude, and Mixed Mode
Format Adjust and Rounding
Parallel Data Load and Passthrough from Input Port
Full 32-Bit Product Output Port
16-Bit Output Multiplexer
Independent Three-State Control for LSP and MSP
Sign, Overflow, and Zero Status Flags
Pin-Compatible with B2018
1.20" Square 108-Pin Grid Array

APPLICATIONS
Digital Signal Processing
Array Processors
Super-Minicomputers
General-Purpose Computing



The ADSP-7018 produces a 32-bit product that may be format-adjusted for consistent signed fractional output format and for maximum precision in a 16-bit MSP. The MSP of the format-adjusted 32-bit product can be rounded with a control which causes a 1 to be added to the Most Significant Bit (MSB) of the LSP. Three status flags indicate the presence of a zero, negative, or overflowed result. The input operands can be loaded and passed directly through without multiplication, but with format adjustment, rounding, and setting of status flags.

The ADSP-7018 is a pin-for-pin replacement for Bipolar Integrated Technology's B2018 TTL 16 × 16 Multiplier.

The ADSP-7018 is available for commercial temperature ranges in a compact, hermetically-sealed 108-pin grid array.

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GENERAL DESCRIPTION

The ADSP-7018 is a high-speed 16 × 16-bit parallel TTL multiplier, fabricated in TTL-compatible oxide-isolated ECL. The ADSP-7018 has two 16-bit input ports and a fielded 32-bit output port. 32-bit products are available in parallel, or the most significant enabled 16-bit Least Significant Product (LSP) and 16-bit Most Significant Product (MSP) portions, or LSP and MSP multiplexed to a single 16-bit port. Each 16-bit field of the product latch has its own three-state output control.

Inputs can be represented in either twos-complement, unsigned-magnitude, or mixed-mode formats. The input, instruction, status, and output latches are all latches which can be enabled to be transparent. Input operands and output results are stored in individually enabled latches with separate clocks for input and output. For unclocked flow-through operation, the latches can be made transparent by holding clocks and enables active. Tying clocks together as a single clock causes input and output latches to operate in complementary fashion, simplifying synchronous operation. The two clocks are fully independent, allowing double clock operation. With both clock lines held active, the three enable controls can function as three independent clock lines for the two data input ports and the output port, respectively.

SPECIFICATIONS[1]

ABSOLUTE MAXIMUM RATINGS

Parameter		ADSP-7018 Min	ADSP-7018 Max	Unit
V_{CC}	Supply Voltage (GND = 0)	−0.5	+7.0	V
V_{IN}	Input Voltage (GND = 0)	−0.5	V_{CC} + 0.5	V
I_O	Output Source Current			
	Continuous		30	mA
	Surge		100	mA
T_{ST}	Storage Temperature (ambient)	−55	+150	°C
T_J	Operating Junction Temperature		+165	°C

RECOMMENDED OPERATING CONDITIONS

Parameter		ADSP-7018 Min	ADSP-7018 Max	Unit
V_{CC}	Supply Voltage	4.75	5.25	V
T_{AMB}	Operating Temperature (ambient)[3]	0	+70	°C

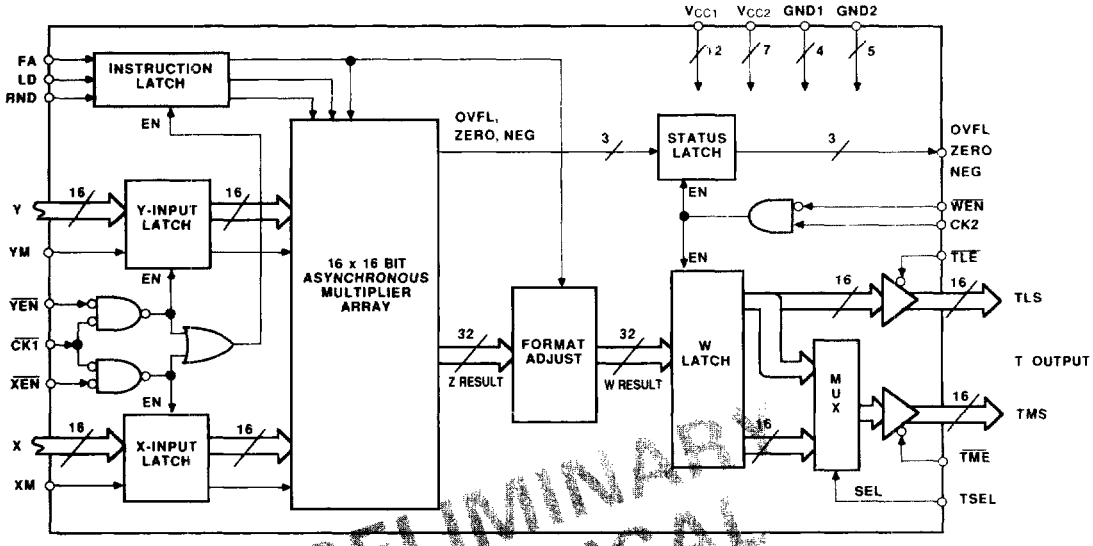
ELECTRICAL CHARACTERISTICS

Parameter		Test Conditions	ADSP-7018 Min	ADSP-7018 Max	Unit
V_{IH}	High-Level Input Voltage	@ V_{CC} = max	2.0		V
V_{IL}	Low-Level Input Voltage	@ V_{CC} = min		0.8	V
V_{OH}	High-Level Output Voltage	@ V_{CC} = min & I_{OH} = max	2.4		V
V_{OL}	Low-Level Output Voltage	@ V_{CC} = min & I_{OL} = max		0.4	V
I_{IH}	High-Level Input Current, All Inputs	@ V_{CC} = max & V_{IN} = 2.4V		200	µA
I_{IL}	Low-Level Input Current, All Inputs	@ V_{CC} = max & V_{IN} = 0.4V		200	µA
I_{OH}	High-Level Output Current			−400	µA
I_{OL}	Low-Level Output Current			4.0	mA
I_{OZ}	Three-State Leakage Current	@ V_{CC} = max; High Z; V_{IN} = 0 or V_{CC} = max		40	µA
I_{CC}	Supply Current	@ V_{CC} = max; max clock rate; TTL inputs		800	mA

SWITCHING CHARACTERISTICS[2]

Parameter		ADSP-7018J Min	ADSP-7018J Max	Unit
t_S	Input Setup Time	4		ns
t_H	Input Hold Time	3		ns
t_C	Clock and Latch Enable Pulse Duration	5.5		ns
t_{DCM}	Data to Clock Multiply Time		14	ns
t_{CCH}	Clock to Clock Hold Time	−1.5		ns
t_{CCM}	Clock to Clock Multiply Time		19	ns
t_{COD}	Clocked Output Delay		12	ns
t_{DDM}	Data to Data Multiply Time		25	ns
t_{CDM}	Clock to Data Multiply Time		26	ns
t_{PHZ}	Output Disable Delay High to HI-Z		7	ns
t_{PHL}	Output Disable Delay Low to HI-Z		7	ns
t_{PZH}	Output Enable Delay HI-Z to High		12	ns
t_{PZL}	Output Enable Delay HI-Z to Low		11	ns

NOTES
[1]All min and max specifications are over power-supply and temperature range indicated.
[2]Input levels are GND and + 3.0V. Rise times are 5ns. Input timing reference levels and output reference levels are 1.5V, except for t_{ENO} and t_{DAO} which are as indicated in Figure 1.
[3]500 linear feet per minute ambient air flow.
Specifications subject to change without notice.



Functional Block Diagram

PIN DESCRIPTION

DATA

X_{15-0}	X Operand Input
Y_{15-0}	Y Operand Input
TMS_{15-0}	MSP of 32-Bit T Output
TLS_{15-0}	LSP of 32-Bit T Output

CONTROL

$\overline{XEN}$	Enable X-Input Latch
$\overline{YEN}$	Enable Y-Input Latch
$\overline{WEN}$	Enable W Latch
XM	X-Input Data Format
YM	Y-Input Data Format
FA	Format Adjust
LD	Load Concatentated X and Y Operands
RND	Round MSP
$\overline{TME}$	Enable TMS Output (Active LO)
$\overline{TLE}$	Enable TLS Output (Active LO)
TSEL	Select MSP or LSP to TMS Port

STATUS

ZERO	Zero
OVFL	Overflow
NEG	Negative

CLOCKS

$\overline{CK1}$	Input Latches Clock
CK2	Output Latches Clock

POWER

V_{CC1}	Positive Supply Voltage to Internal Logic
V_{CC2}	Positive Supply Voltage to Output Circuits
GND1	Negative Supply Voltage to Internal Logic
GND2	Negative Supply Voltage to Output Circuits

METHOD OF OPERATION

The X-Input Latch holds its most recent contents unless $\overline{CLK1}$ is LO (logic 0) when enabled (made transparent) by $\overline{XEN}$ also LO. Similarly, the Y-Input Latch holds its most recent contents unless $\overline{CLK1}$ is LO when enabled by $\overline{YEN}$ also LO. The state of the $\overline{CK1}$ input clock has no effect on each input latch unless the input enable lines $\overline{XEN}$ and $\overline{YEN}$ are LO, respectively. When these enable lines are LO, the respective latches will pass data when the $\overline{CK1}$ input is LO and hold data when the $\overline{CK1}$ input is HI (logic 1).

The X and Y input data can be either in twos-complement, unsigned-magnitude, or mixed-mode formats (Table I). Twos-complement input data is indicated by HI levels on the XM line for X input data and HI levels on the YM line for Y input data. Unsigned-magnitude X and Y inputs are indicated by LO levels on the XM and YM lines, respectively. Outputs will be in the same format as inputs unless the input formats are mixed, in which case the outputs will be in twos-complement representation. XM and YM are latched into the X-Input and Y-Input Latches with the input operand data.

The Instruction Latch holds its most recent contents unless $\overline{CLK1}$ is LO when enabled by *either* $\overline{XEN}$ *or* $\overline{YEN}$ also LO. When $\overline{CK1}$ is HI, the contents of the Instruction Latch will be held. If both $\overline{XEN}$ and $\overline{YEN}$ are HI, the contents of the Instruction Latch will also be held. Round (RND), format adjust (FA), and load (LD) are the three instruction bits that pass through or are held at the Instruction Latch.

The ADSP-7018's W output is fielded into a 16-bit most significant product (MSP) and a 16-bit least significant product (LSP). When the RND is HI, the MSP of the W result will be rounded by adding a binary 1 (with carry) to the most significant bit (MSB) of the LSP, consistently rounding toward positive infinity at mid-scale. Truncating the MSP (RND LO) introduces a large-sample statistical bias of $-(2^{16}-1)/2$ LSBs of the LSP, while rounding (RND HI) reduces the bias to $+1/2$ LSBs of the LSP.

The FA control format adjusts the Z output from the multiplier array. When FA is HI, the full 32-bit Z result is passed unmodified to the W latch (Tables II and III). All possible products can be represented without overflow, including twos-complement fractional $(-1.0) \times (-1.0)$. The binary point in the MSP of a twos-complement fractional product will not align with the binary point in the input operands. Thus, the numeric weighting of data within a system using this format (with FA HI) will not be uniform. Also, the two highest-order bits in a twos-complement product are normally redundant. An additional bit of precision in the MSP could be obtained by eliminating one of these redundant bits.

Format adjust (FA LO) shifts the Z result left by one bit position and right-fills a binary zero (Table III). Thus, format adjust eliminates redundant high-order bits in twos-complement products. The MSPs of fractional twos-complement products also receive proper weighting relative to input data. However, an overflow on format adjust will occur when full-scale negative is multiplied by itself, yielding full-scale negative instead of the correct positive product (which is not representable in format-adjusted twos-complement format). This special condition is monitored by the OVFL flag so that it does not go undetected.

The Load (LD) instruction determines whether the multiplier array is active or put into a pass-through mode. When LD is LO, the multiplier array is active and produces the product of the X and Y input values as Z result. When LD is HI, the multiplier array is put in the pass-through mode and the X and Y input values are concatenated to form a Z result with the X input in the most significant position (Table II). XM determines the sign mode of the complete 32-bit Z result. ZERO, OVFL and NEG are set depending on the value of this Z result. RND and FA can also be used in this mode. Load allows any 32-bit number loaded through the input ports to be rounded, tested for zero and sign, and to have fractional binary points aligned while testing for overflow. It is also valuable for system testing by providing a direct path through the multiplier and greater access to latches within the ADSP-7018.

Output flags ZERO, OVFL, and NEG are generated from the intermediate Z result. When not rounding (RND LO), ZERO is set when the full 32-bit result is zero. When rounding (RND HI), ZERO is set when the format-adjusted MSP in the W result will be zero. That is, when rounding, ZERO is set for $Z_{31\text{-}16}$ equals zero when FA HI but ZERO is set for $Z_{31\text{-}15}$ equals zero when FA LO. Zero will not be set if an overflow condition exists.

OVFL is set only for twos-complement multiplications of full-scale negative times full-scale negative when format adjusting (FA LO).

NEG is set only when a twos-complement or mixed-mode Z result is negative. A loaded, previously overflowed result (MSB of 1 followed by all zeros) will set NEG as well as OVFL, if loaded with XM HI.

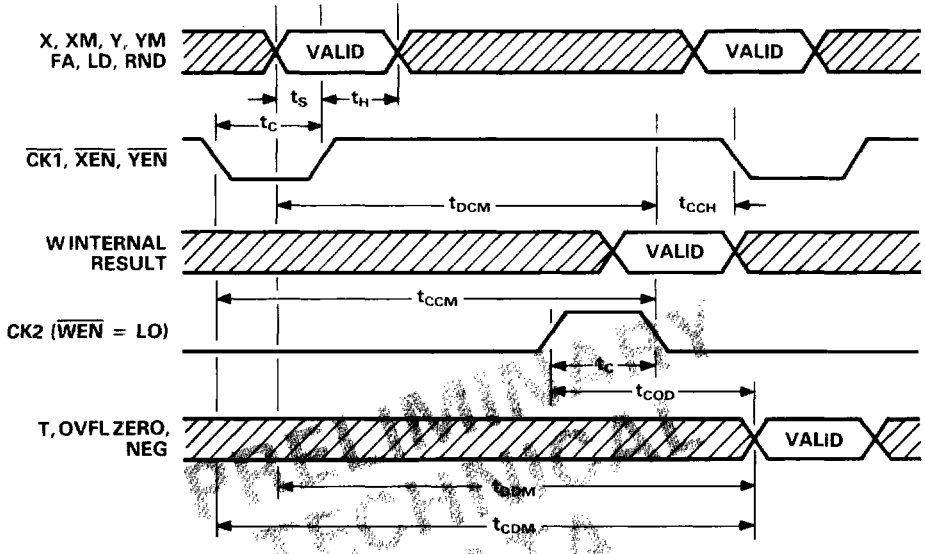
The output latches for data and flags ZERO, OVFL and NEG hold their most recent contents unless CLK2 is HI when enabled by $\overline{WEN}$ LO. With $\overline{WEN}$ LO, the output latches are transparent when CK2 is HI and data is held when CK2 is LO. The ADSP-7018 can be made a totally asynchronous device by holding all enables active ($\overline{XEN}$, $\overline{YEN}$, and $\overline{WEN}$ all LO) and $\overline{CLK1}$ LO and CLK2 HI. Note that the clock definitions are complementary; if $\overline{CLK1}$ and CLK2 are tied together and enable lines asserted, input latches will be transparent when output latches are latched and vice versa. $\overline{CLK1}$ and CLK2 are fully independent, allowing double-clock operation. For triple-clock operation, the two clock lines can be held active which causes the three latch enable controls to behave like independent clock lines.

The T output is fielded into two 16-bit portions, TMS and TLS, each with its own three-state controls. A HI on the asynchronous $\overline{TME}$ or $\overline{TLE}$ lines disables the corresponding TMS or TLS output driver to a high-impedance state. Conversely, a LO on $\overline{TME}$ or $\overline{TLE}$ enables the corresponding output driver, driving the output bus.

TSEL controls the multiplexer feeding the TMS field (Table IV). When TSEL is LO, the MSP from the W Latch will be passed to the TMS output. When TSEL is HI, the LSP will be routed to TMS. This multiplexer and its associated TSEL control simplifies operation of the ADSP-7018 in 16-bit bus systems.

TTL 16 × 16-BIT FIXED-POINT MULTIPLIER

CLOCKED AND UNCLOCKED TIMING



NOTE: FOR FLOWTHROUGH OPERATION, THE LATCHES MUST BE MADE TRANSPARENT.

OUTPUT ENABLE

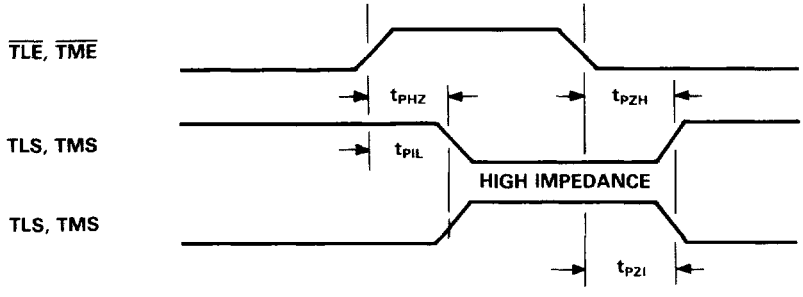


Figure 1. ADSP-7018 Timing Diagram

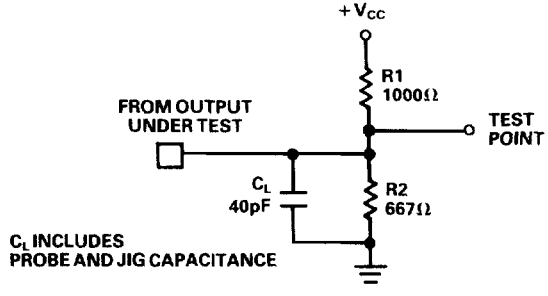


Figure 2. ADSP-7018 Load Test Circuit

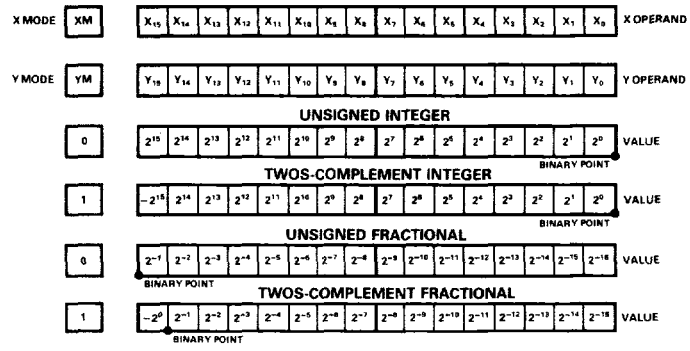
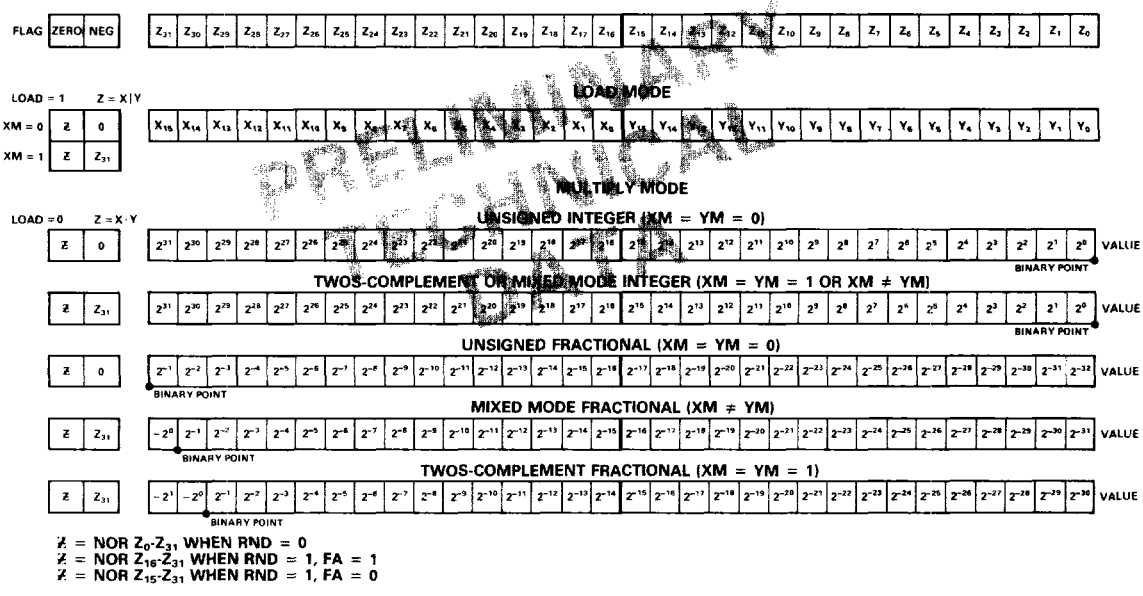


Table I. ADSP-7018 Input Data Formats



Z = NOR Z_0-Z_{31} WHEN RND = 0
Z = NOR Z_{16}-Z_{31} WHEN RND = 1, FA = 1
Z = NOR Z_{15}-Z_{31} WHEN RND = 1, FA = 0

Table II. ADSP-7018 Z Result Formats, ZERO and NEG Flags, and Load Operation

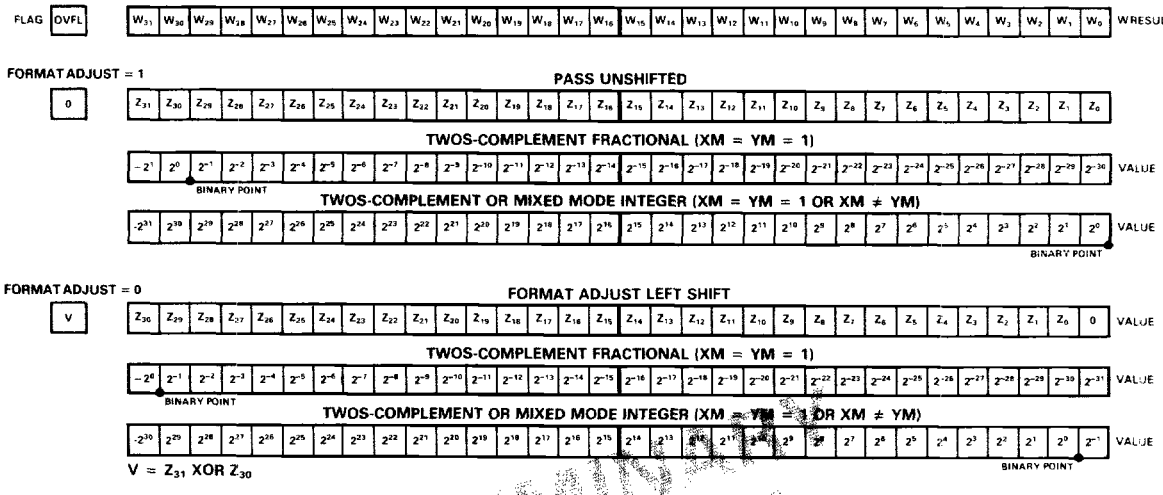


Table III. ADSP-7018 W Result Formats, OVFL Flag, and Format Adjust Operation

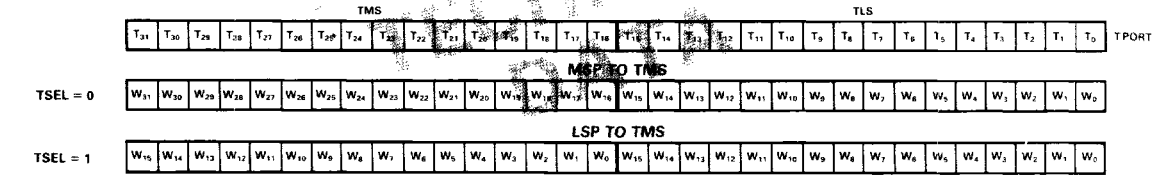


Table IV. ADSP-7018 Output Multiplexer

ORDERING INFORMATION

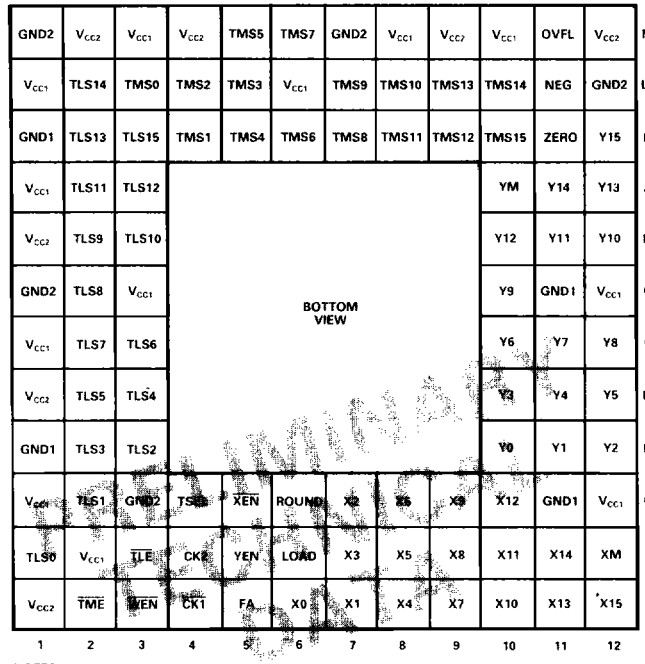
Part Number	Temperature Range	Package	Package Outline
ADSP-7018JG	0 to +70°C	108-Pin Grid Array	G-108A

ESD SENSITIVITY

The ADSP-7018 features input protection circuitry consisting of large "distributed" diodes and polysilicon series resistors to dissipate both high-energy discharges (Human Body Model) and fast, low-energy pulses (Charged Device Model). Per Method 3015.2 of MIL-STD-883C, the ADSP-7018 has been classified as a Category A device.

Proper ESD precautions are strongly recommended to avoid functional damage or performance degradation. Charges as high as 4000 volts readily accumulate on the human body and test equipment and discharge without detection. Unused devices must be stored in conductive foam or shunts, and the foam should be discharged to the destination socket before devices are removed. For further information on ESD precautions, refer to Analog Devices' ESD Prevention Manual.

ADSP-7018 PIN CONFIGURATION



NOTES
1. ALL V_{CC1} PINS MUST BE TIED TO ALL V_{CC2} PINS.
2. ALL GND1 PINS MUST BE TIED TO ALL GND2 PINS